

Course Design of Computer Organization

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topics

- 1. Verilog and Xilinx ISE
- 2. Basic logic component of datapath design
- 3. ALU and the ALU controller design
- 4. R-type instruction processor design
- 5. CPU controller design
- 6. Single clock-cycle CPU design
- 7. Multiple clock-cycle clock CPU design
- 8. Microprogrammed CPU controller unit design
- 9. Design of datapath of Microprogrammed CPU

Outline

- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures

Experiment Purpose

- Understand the principles of Microprogrammed Multiple clock-cycle CPU Controller
- Master design methods of Microprogram Controller
- Master methods of program verification of Microprogrammed CPU Controller

Experiment Task

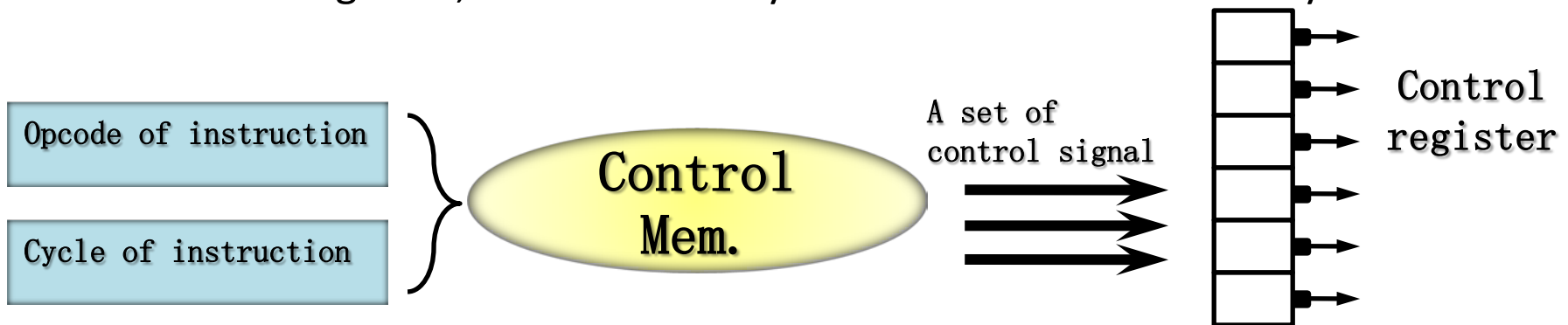
- Design the Microprogram Controller.
- Verify the State Diagram of Microprogram Controller.

Basic Principle

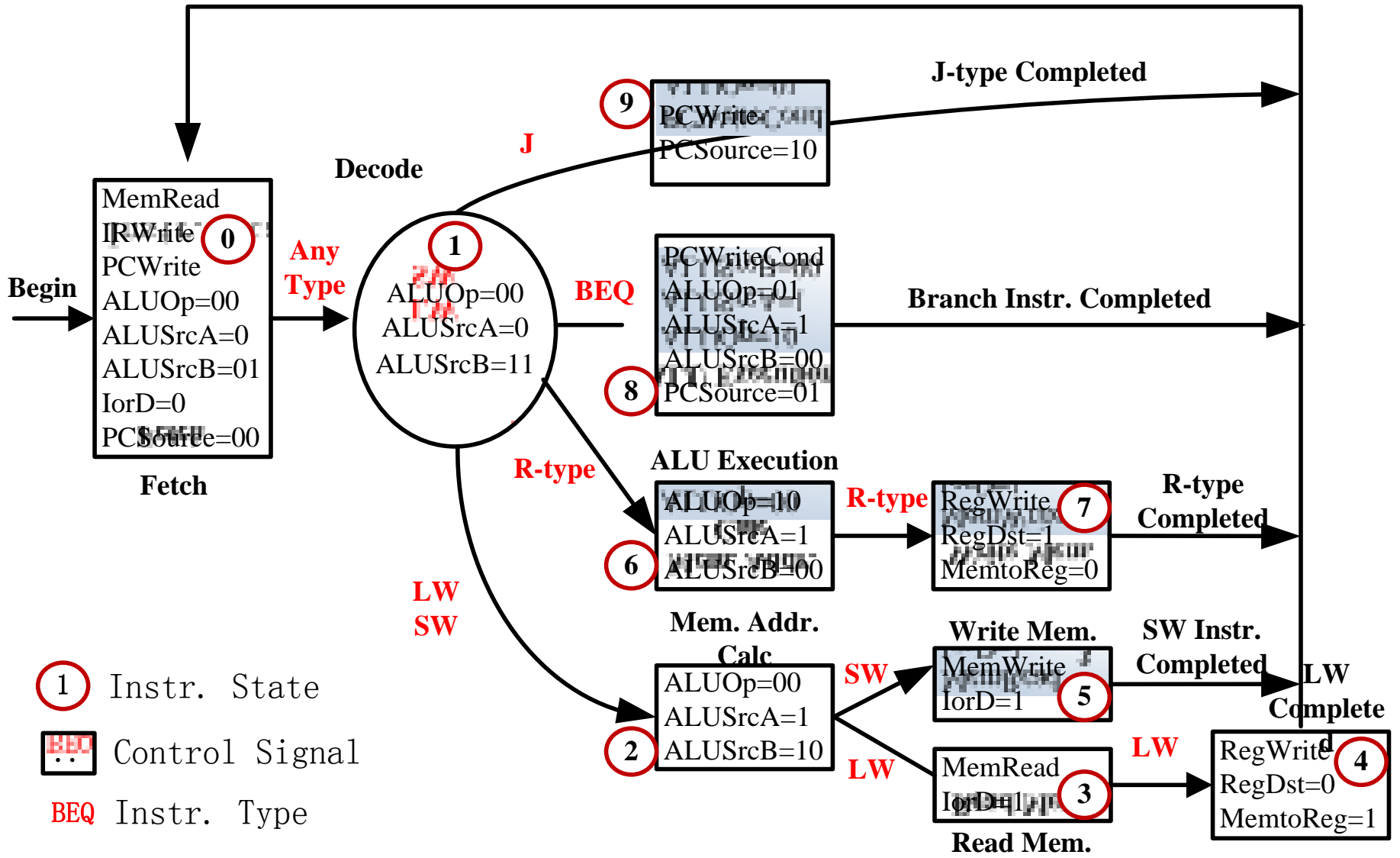
- Microprogrammed Control
- Microprogram Control State Diagram

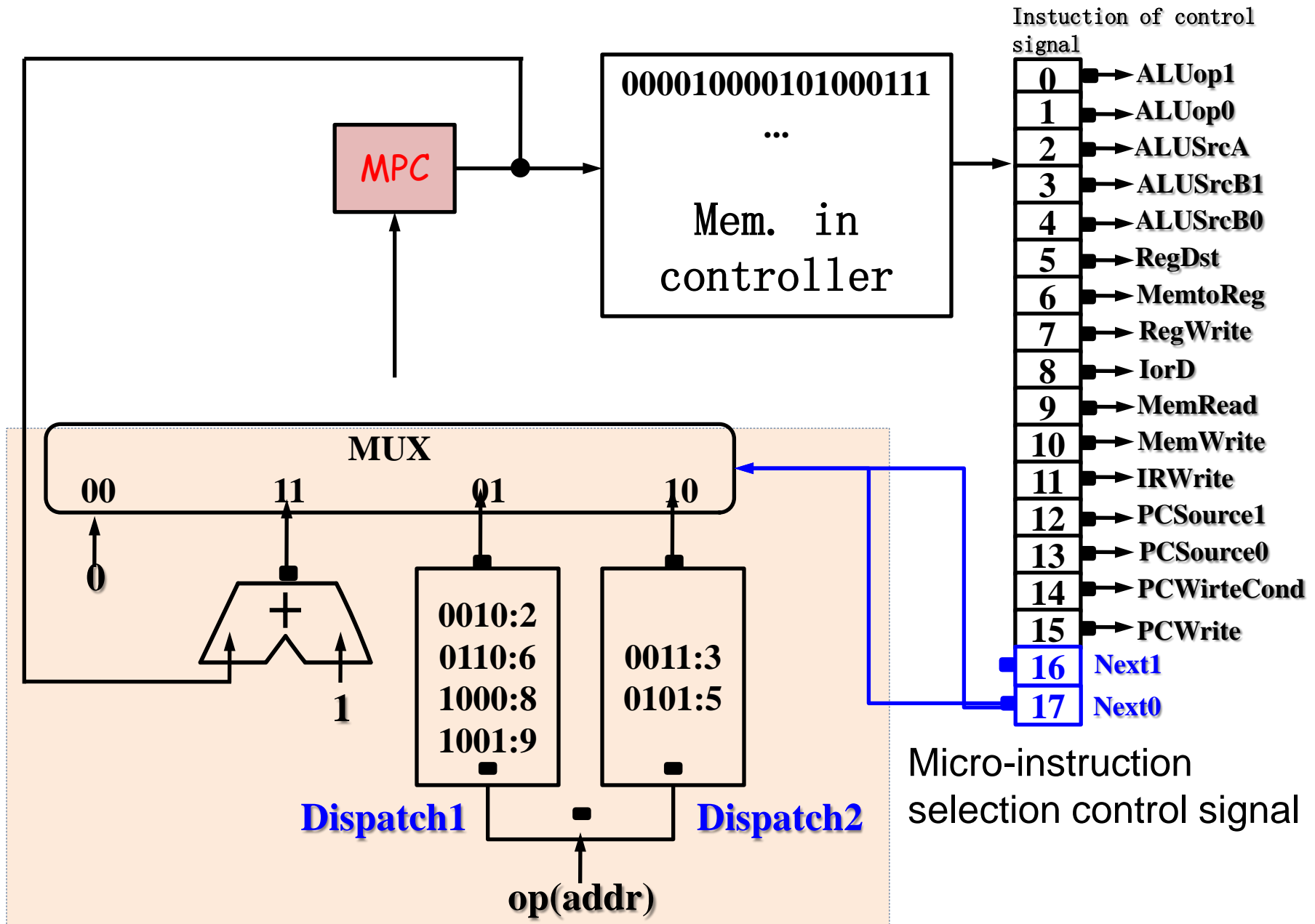
Microprogram Control

- Multi-cycle CPU, all the control signals can be located under the instruction operation code and current state, by combinational logic circuit, resulting in all the control signals.
- microprogram, means putting control signal in all of its clock cycles per instruction together, stored in binary form in the control memory



- Multiple clock-cycle, each state corresponds to a group of control signals (*micro-instruction*)
- Each Instruction has a series of the control signal sets corresponding to one group (*microprogram*)
- Store the mico-instructions in the control Mem. in order





Next	operating	MPC
00	Begin a new instruction	MPC = 0
11	Running next micro-instruction in order	MPC += 1
01	The first level micro-instruction branch	According to opcode
10	The second level micro-instruction branch	

#	Tags	ALU			Register	Memory	PC	Next	Control signal
		OP	A	B					PPABBRMGIRWTSSCPNN
0	Fetch	Add	PC	4		ReadPC	ALU	Seq	0x0851 2'b11
1		Add	PC	ExtSft	Read			Dispatch1	0x1800 2'b01
2	MEM1	Add	A	Ext				Dispatch2	0x3000 2'b10
3	LW2					ReadALU		Seq	0x0060 2'b11
4					WriteMDR			Fetch	0x0300 2'b00
5	SW2					WriteALU		Fetch	0x00A0 2'b00
6	Rf1	Func	A	B				Seq	0xA000 2'b11
7					ALUout			Fetch	0x0500 2'b00
8	BEQ1	Sub	A	B			ALUCond	Fetch	0x6006 2'b00
9	J1						Jump		0x0009 2'b00

address	Control signal-CM	
	PPABBRMGIRWTSSCPNN	
0	0x0851 2'b11	0000 1000 0101 0001 11
1	0x1800 2'b01	0001 1000 0000 0000 01
2	0x3000 2'b10	0011 0000 0000 0000 10
3	0x0060 2'b11	0000 0000 1100 0000 11
4	0x0300 2'b00	0000 0011 0000 0000 00
5	0x00A0 2'b00	0000 0000 1010 0000 00
6	0xA000 2'b11	1010 0000 0000 0000 11
7	0x0500 2'b00	0000 0101 0000 0000 00
8	0x6006 2'b00	0110 0000 0000 0110 00
9	0x0009 2'b00	0000 0000 0000 1001 00

branch-ROM1		
address	value	instruction
0	2	LW/SW
1	6	R
2	8	BEQ
3	9	J

branch-ROM2		
address	value	instruction
0	3	LW
1	5	SW

Experiment Content

- To simplify the design, we use state machine instead of control unit Mem..
- Testing 18-bit control signal of R、 LW、 SW、 BEQ、 J
 - first16-bit of micro-instructions per instruction control signals, require hexadecimal display in the 4 seven-segment LED tube or simulation waveform diagram
 - Last 2-bit of micro-instructions, require display in 2 LED lamp.
- Program to Spartan-3 Board and verify 5 types Instruction.

Thanks!