Course Design of Computer Organization

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topics

- 1. Verilog and Xilinx ISE
- 2. Basic logic component of datapath design
- 3. ALU and the ALU controller design
- 4. R-type instruction processor design
- 5. CPU controller design
- 6. Design of datapath of single-cycle clock CPU
- 7. Multiple-cycle clock CPU design
- 8. Microprogrammed CPU controller unit design
- 9. Design of datapath of Microprogrammed CPU

Outline

- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures

Experiment Purpose

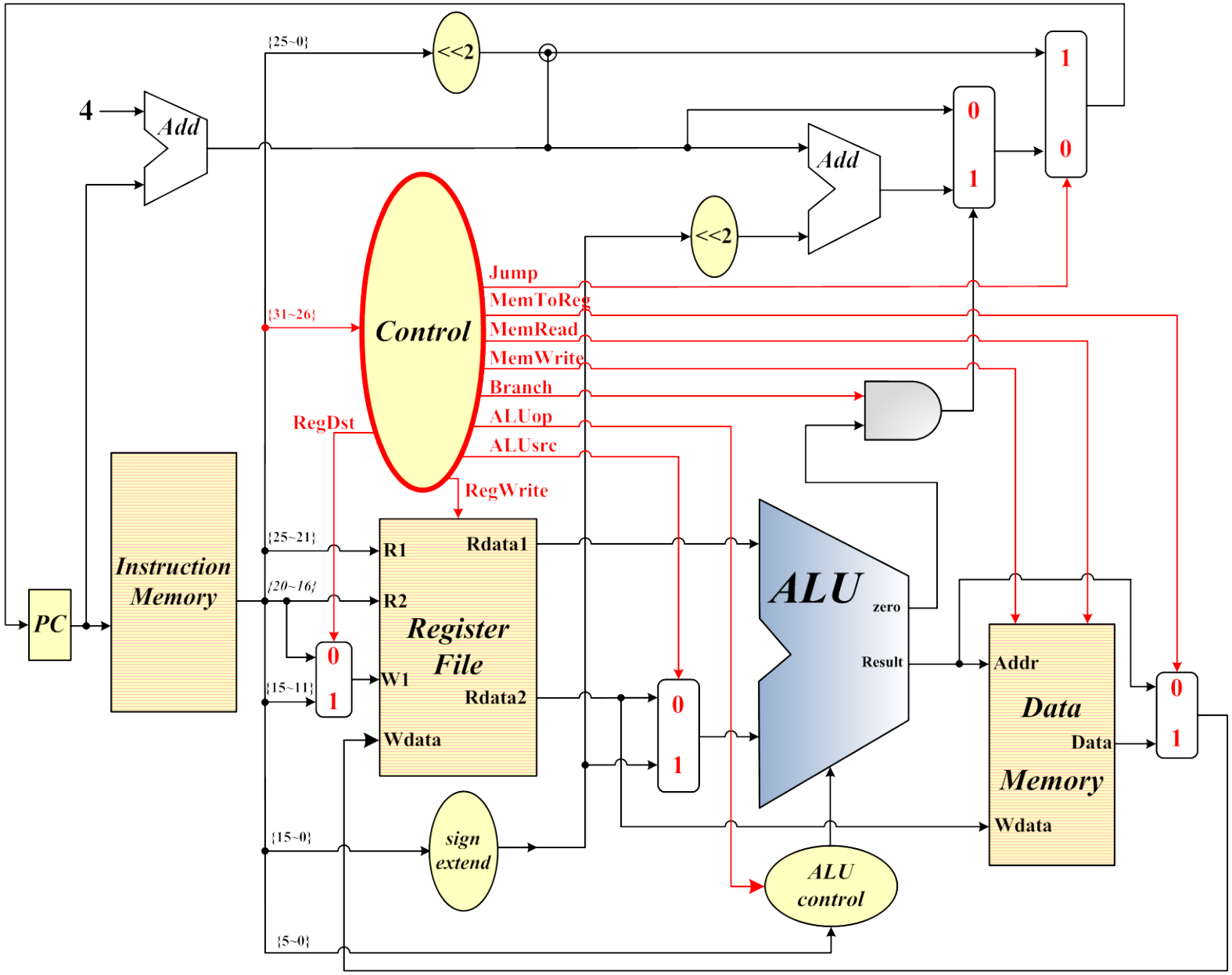
- Understand the working principles and functions of CPU Controller.
- Master the design method of CPU controller.

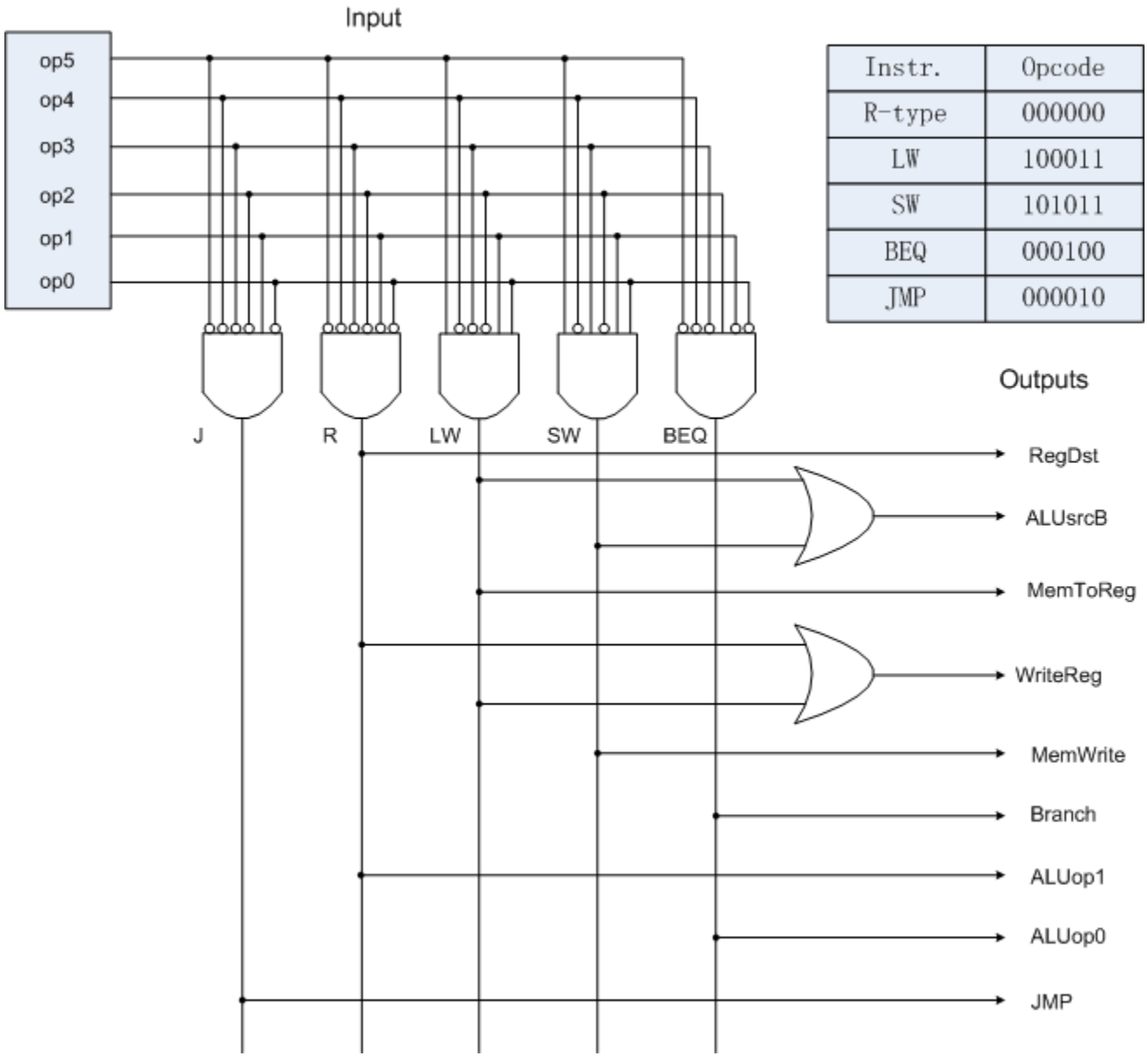
Experiment Task

- Realize a single-clock CPU controller which can execute R-type, LW, SW, BEQ and JMP instruction, then simulate it and verify it by FPGA.

Basic Principle

- The function of CPU Controller.
- The input and output of CPU Controller.


4
Add
{25~0}
<<2
Add
<<2
1
0
0
1
Control
Jump
MemToReg
MemRead
MemWrite
Branch
ALUop
ALUsrc
RegWrite
RegDst
{31~26}
PC
Instruction Memory
{25~21}
{20~16}
{15~11}
R1
R2
W1
Wdata
Rdata1
Rdata2
Register File
0
1
0
1
ALU
zero
Result
Addr
Data
Memory
Data
Wdata
0
1
{15~0}
sign extend
{5~0}
ALU control



Instr.	Opcode
R-type	000000
LW	100011
SW	101011
BEQ	000100
JMP	000010

Experiment Content

- 1. Implement the CPU Controller module.
- 2. Implement Verilog Test Fixture module, assign 5 type instructions to opcode in “initial” segment.
- 3. Write UCF file: 6-bit opcode is associated with 6 switch buttons, 9-bit output is associated with 8 LED lamps and 1 dot of tubes.
- 4. Program the bit file and verify it.